App. Serial No. 10/598,755 Docket No.: NL040276US1

Remarks

In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

The non-final Office Action dated April 17, 2008, lists the following rejections: claims 1-7 and 9-11 stand rejected under 35 U.S.C. § 103(a) over An *et al.* (U.S. Patent No. 6,245,618) in view of Wu (U.S. Patent No. 5,773,348); claim 8 stands rejected under 35 U.S.C. § 103(a) over An and Wu in further view of Lai (U.S. Patent Pub. 2002/0102801). The Office Action also asserts that the title of the invention is not descriptive, that an amendment to the Specification is required to correct a typographical error, and that claim 7 requires a typographical correction.

Applicant respectfully traverses the § 103(a) rejections of claims 1-11 because the cited combination does not correspond to the claimed invention which includes, for example, aspects directed to performing an amorphizing implantation prior to performing two implantations of dopants of opposite conductivity types. The Office Action acknowledges that the An reference does not disclose such aspects of the claimed invention. See, e.g., page 4:18-21 of the instant Office Action. The Office Action then erroneously asserts that the cited portions of the Wu reference teach performing an amorphizing implantation before performing two implantations of dopants of opposite conductivity type. As a first example, the Office Action inaccurately asserts that Wu's doped region 28 is formed by an amorphizing implantation. The cited portions of Wu, however, do not teach that doped region 28 is formed by an amorphizing implantation. See, e.g., Figure 4 and Col. 4:25-39. As a second example, the Office Action mischaracterizes the cited portions of Wu as teaching that lightly-doped areas 36 and heavily-doped areas 42 are formed by two implantations of dopants of opposite conductivity type. In actuality, the cited portions of Wu teach that lightly-doped areas 36 (i.e., N lightly-doped areas in the source and the drain regions of the MOS device) and heavily-doped areas 42 (i.e., N⁺ heavily-doped areas of the source and the drain of the MOS device) are formed by implantations of dopants of the same conductivity type. See, e.g., Figures 9-11 and Col. 5:38-50. Thus, the Office Action fails to cite to any reference that teaches performing an amorphizing implantation prior to performing two implantations of dopants of opposite conductivity type as in the claimed invention.

App. Serial No. 10/598,755 Docket No.: NL040276US1

implantations of dopants of opposite conductivity type as in the claimed invention. Accordingly, the § 103(a) rejections of claims 1-11 are improper and Applicant requests that they be withdrawn.

Applicant further traverses the § 103(a) rejection of claim 7 because the cited combination does not correspond to aspects of the claimed invention directed to annealing the first and second implantations at a temperature between 500 and 600°C. The Office Action acknowledges that the An reference does not disclose such aspects of the claimed invention. See, e.g., page 4:18 to page 5:2 of the instant Office Action. The Office Action then erroneously asserts that the cited portions of the Wu reference teach annealing first and second implantations of dopants of different conductivity types at a temperature between 500 and 600°C. The cited portions of Wu, however, as discussed above, teach that lightly-doped areas 36 and heavily-doped areas 42 (i.e., the areas formed by the Office Action's alleged first and second implantations) are formed by implantations of dopants of the same conductivity type. See, e.g., Figures 9-11 and Col. 5:38-50. Moreover, the cited portions of Wu teach that the first annealing process, which is performed at a temperature between 400 and 650°C (i.e., the Office Action's alleged annealing step), transforms amorphous silicon 34a, which is a deposited layer (see, e.g., Figure 6 and Col. Col. 4:64-66), into polysilicon. See, e.g., Col. 6:3-11. Wu further teaches that it is the second annealing step, which is performed at a temperature between 750 and 900°C, that serves to drive-in the trapped atoms implanted in Figure 10 to form the heavily-doped areas 42 of the source and drain. See, e.g., Col. 6:5-14. Thus, the cited portions of Wu teach annealing the Office Action's alleged first and second implantations at a temperature between 750 and 900°C. As such, the Office Action fails to cite to any reference that teaches annealing the first and second implantations at a temperature between 500 and 600°C as in the claimed invention. Accordingly, the § 103(a) rejection of claim 7 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the Office Action's assertion that the title of the invention is not descriptive. The claimed invention is directed to a method of manufacturing a semiconductor device as is indicated by the title. As such, Applicant submits that the title of the invention is descriptive of the invention claimed in compliance with M.P.E.P. §§ 606 and 606.01.

App. Serial No. 10/598,755 Docket No.: NL040276US1

In response to the objection to the specification and claim 7, Applicant has replaced "en" with "and' in both instances. Thus, Applicant requests that the objections be removed.

Applicant notes that minor amendments have been made to clams 1-11 to remove unnecessary reference characters and to improve readability in view of the removal of these reference characters. These amendments are not being made to overcome any of the rejections raised by the Office Action, which fail for at least the reasons discussed above.

Applicant has also added new claims 12-19. Applicant submits that claims 12-19 are allowable over the cited references for at least the reasons discussed above relating to the impropriety of the § 103(a) rejection of claim 1.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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